Investigating Data Propagation Strategies for Switch Routing Features

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ABSTRACT

The conceptual model of a router is quite straightforward: a router has a data path and a control path. The job of the data path is to move packets that arrive on input or ingress ports to output or egress ports; from the outputs, these packets are sent on downstream to the next switch on the path or to an end-host. Routers are a great example of special-purpose computers built for a specific set of tasks. Routers are big business: according to some market research firms, worldwide revenue from enterprise and service provider router sales. In this paper, we provide an up-to-date knowledge of high-speed network. with the basic concepts, the architectures, the protocols, the advantages and limitations, and the recent development of various high-speed networking technologies with two fundamental issues need to be addressed to make this architecture sensible by the two points i.e.; how to minimize the overhead of an individual packet buffer; and how to design scalable packet buffers using independent buffer subsystems. We address these issues by first designing an efficient compact buffer that reduces the SRAM size requirement by (k - 1)/k. after that we introduce a feasible way of coordinating multiple subsystems with a load-balancing algorithm that maximizes the overall system performance. Both experimental results and theoretical analysis exhibits that our load-balancing algorithm and the distributed packet buffer architecture can easily scale to connect the buffering needs of high

bandwidth links and achieve the requirements of scale and support for multiple queues in data routing system

1. INTRODUCTION

THE phenomenal growth of the Internet has been fueled by the rapid increase in the communication link bandwidth. Internet routers play a crucial role in sustaining this growth by being able to switch packets extremely fast to keep up with the growing bandwidth (line rate).This demands sophisticated packet switching and buffering techniques. Packet buffers need to be designed to support large capacity, multiple queues, and provide short response times. The router buffer sizing is still an open issue. The traditional rule of thumb for Internet routers states that the routers should be capable of buffering RTT_R data,where RTT is a round-trip time for flows passing through the router, and R is the line rate. In the author claimed that the size of buffers in backbone routers can be made very small at the expense of a small loss in throughput. Focusing on the performance of individual TCP flows, the author claimed in that the output/input capacity ratio at a network link largely determines the required buffer size. If the output/input capacity ratio is lower than one,the loss rate follows a power-law reduction with the buffer size and significant buffering is needed. Given everlasting controversy, nowadays, routers manufacturers still seem to favor the use of large buffers. For instance, the Cisco CRS-1 modular service card with a 40 Gbps line rate incorporates a 2 GB packet buffer memory per line card .In order to support fine-grained IP quality of service (QoS) requirements, nowadays, a packet buffer usually maintains thousands of queues. For example, the Juniper E-series routers maintain as many as 64,000 queues. Given the increasing popularity of OpenFlow, a packet buffer that supports millions of queues is always desired. Furthermore, a packet buffer should be capable of sustaining continuous data streams for both ingress and regress. With the ever-increasing line rate, current available memory technologies, namely SRAM or DRAM alone cannot simultaneously satisfy these three requirements. This prompted researchers to suggest hybrid SRAM/DRAM (HSD) architecture with a single DRAM, interleaved DRAMs or parallel DRAMs sandwiched between SRAMs.In this paper, we briefly review previous work on packet buffer architectures and present scalable and efficient hierarchical packet buffer architecture. This is our first attempt to combine the merits of two previously published packet buffer

architectures Consequently, the SRAM occupancy has been significantly reduced. By fully exploring the advantage of parallel DRAMs, we first propose a memory management algorithm (MMA) called Random Round Robin (RRR). Thereafter, we devise a "traffic-aware" approach which aims to provide different services for different types of data streams. This approach further reduces the system overhead. Both mathematical analysis and simulation demonstrate that the proposed architecture together with its algorithm reduce the overall SRAM requirement significantly while providing guaranteed performance in terms of low time complexity, upper bounded drop rate, and uniform allocation of resources. In one simulation, the proposed architecture reduces the size of SRAM by more than 95 percent and the maximal delay is only us-level, when the traffic intensity is 76 percent.

1.2 Data Propagation:

Data Propagation is the distribution of data from one or more source data warehouses to one or more local access databases, according to propagation rules. Data warehouses need to manage big bulks of data every day. A data warehouse may start with a few data, and starts to grow day by day by constant sharing and receiving from various data sources.

As data sharing continues, data warehouse management becomes a big issue. Database administrators need to manage the corporate data more efficiently and in different subsets, groupings and time frames. As a company grows further, it may implement more and more data sources especially if the company expansions goes outside its current geographical location.

Data warehouses, data marts and operational data stores are becoming indispensable tools in today's businesses. These data resources need to be constantly updated and the process of updating involves moving large volumes of data from one system to another and forth and back to a business intelligence system. It is common for data movement of high volumes to be performed in batches within a brief period without sacrificing performance of availability of operation applications or data from the warehouse.

2. LITERATURE SURVEY

We have frequently referred to the routing algorithm as the network layer protocol that guides packets through the communication subnet to their correct destination. The times at which routing decisions are made depend on whether the network uses datagrams or virtual circuits. In

a datagram network, two successive packets of the same user pair may travel along different routes, and a routing decision is necessary for each individual packet .In a virtual circuit network, a routing decision is made when each virtual circuit is set up. The routing algorithm is used to choose the communication path for the virtual circuit. All packets of the virtual circuit subsequently use this path up to the time that the virtual circuit is either terminated or rerouted for some reason Routing in a network typically involves a rather complex collection of algorithms that work more or less independently and yet support each other by exchanging services or information. The complexity is due to a number of reasons. First, routing requires coordination between all the nodes of the subnet rather than just a pair of modules as, for example, in data link and transport layer protocols. Second, the routing system must cope with link and node failures, requiring redirection of traffic and an update of the databases maintained by the system. Third, to achieve high performance, the routing algorithm may need to modify its routes when some areas within the network become congested. The main emphasis will be on two aspects of the routing problem. The first has to do with selecting routes to achieve high performance. we discuss algorithms based on shortest paths that are commonly used in practice. we describe sophisticated routing algorithms that try to achieve near optimal performance. The second aspect of routing that we will emphasize is broadcasting routing-related information (including link and node failures and repairs) to all network nodes. This issue and the subtleties associated with it are examined The introductory sections set the stage for the main development. The remainder of this section explains in nonmathematical terms the main objectives in the routing problem and provides an overview of current routing practicepresent some of the main notions and results of graph theory, principally in connection with shortest paths and minimum weight spanning trees. uses the material on graph theory to describe methods for topological design of networks. Finally, the routing system of the Codex network and its relation to the optimal routing algorithm

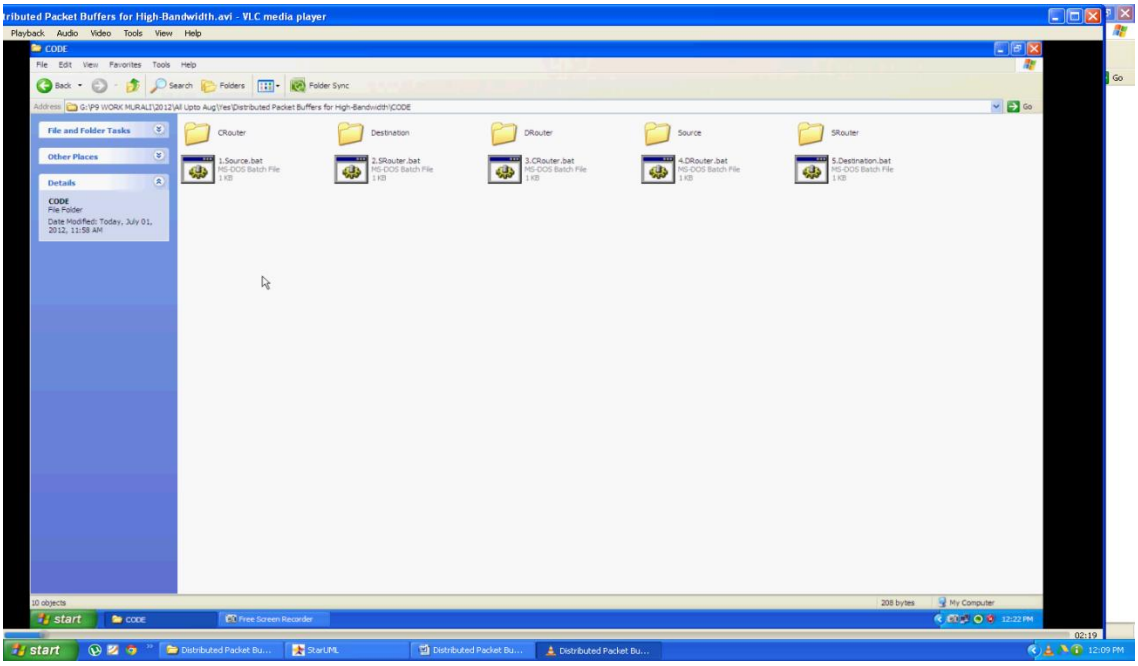
3. PROBLEM STATEMENT

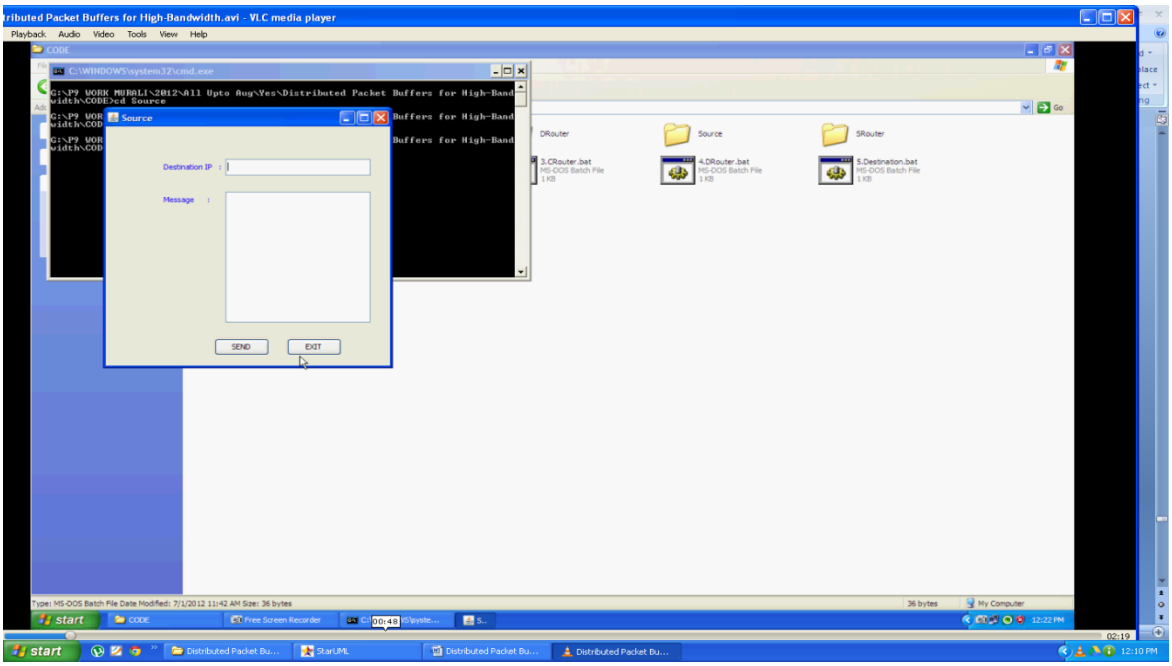
The router buffer sizing is still an open issue. The traditional rule of thumb for Internet routers states that the routers should be capable of buffering RTT*R data, where RTT is a round-trip time for flows passing through the router, and R is the line rate. Many researchers claimed that the size of buffers in backbone routers can be made very small at the expense of a small loss in throughput. Focusing on the performance of individual TCP flows, researchers claimed that the output/input capacity ratio at a network link largely determines the required buffer size. If the output/input capacity ratio is lower than one, the loss rate follows a power-law reduction with the buffer size and significant buffering is needed

4. PROPOSED SYSTEM

We devise a "traffic-aware" approach which aims to provide different services for different types of data streams. This approach further reduces the system overhead. Both mathematical analysis and simulation demonstrate that the proposed architecture together with its algorithm reduce the overall SRAM requirement significantly while providing guaranteed performance in terms of low time complexity, upper bounded drop rate, and uniform allocation of resources.

5. SCREENSHOTS & RESULTS

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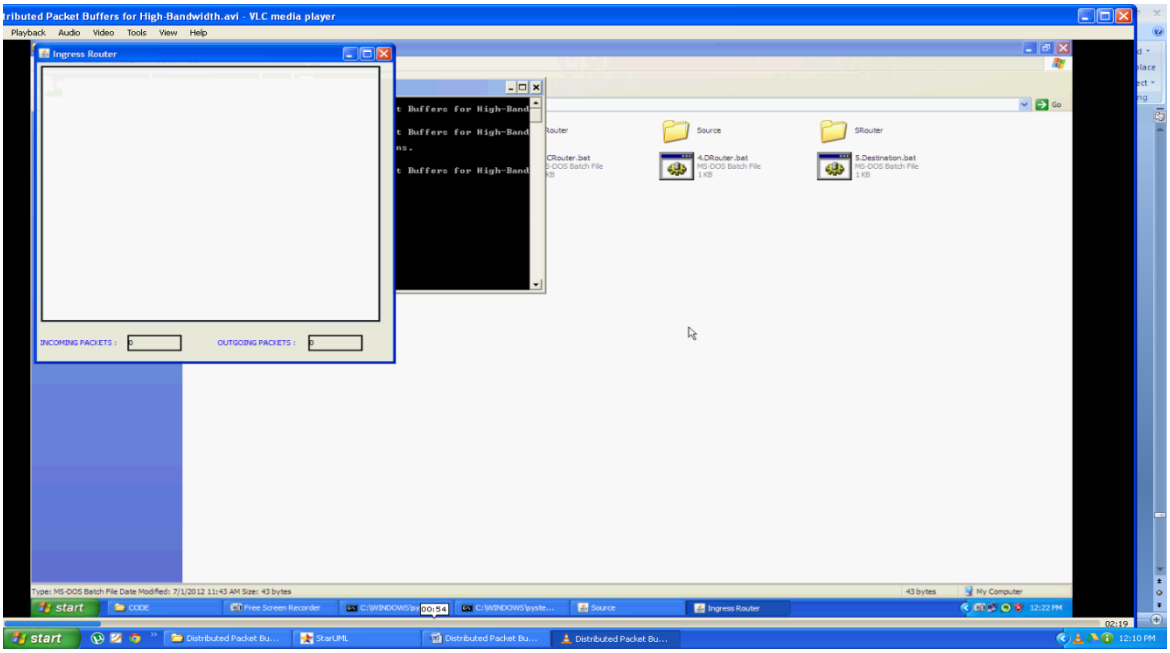
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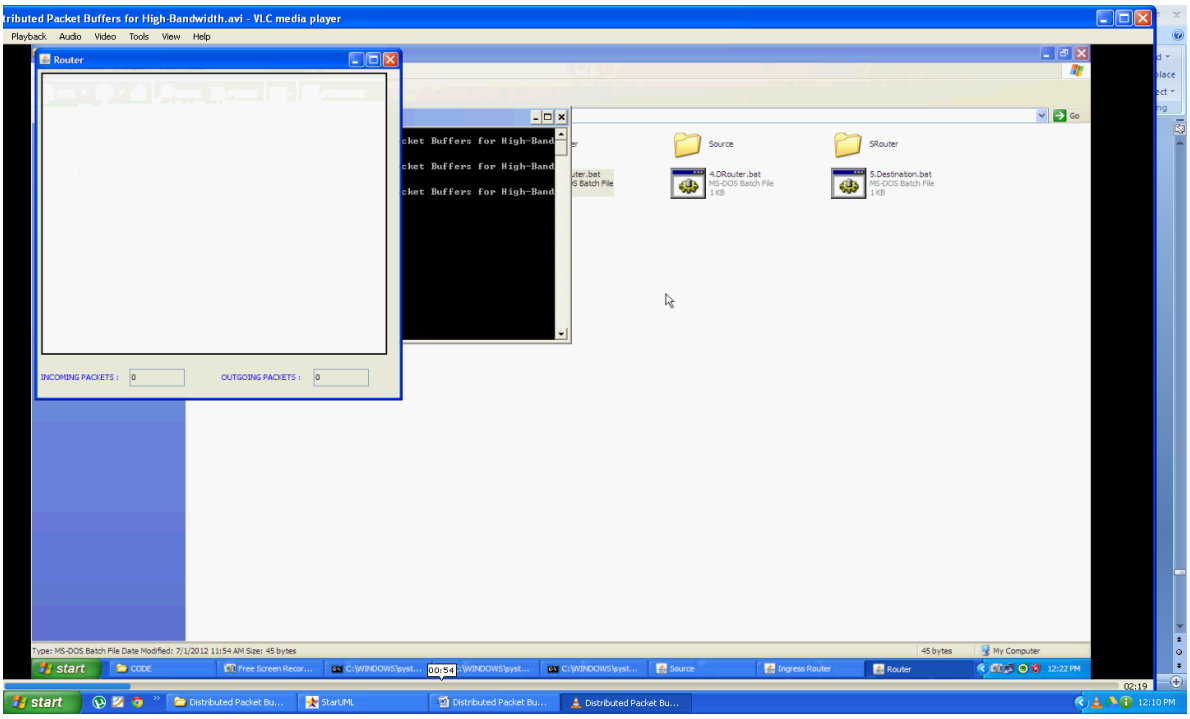
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1 KB
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1 KB
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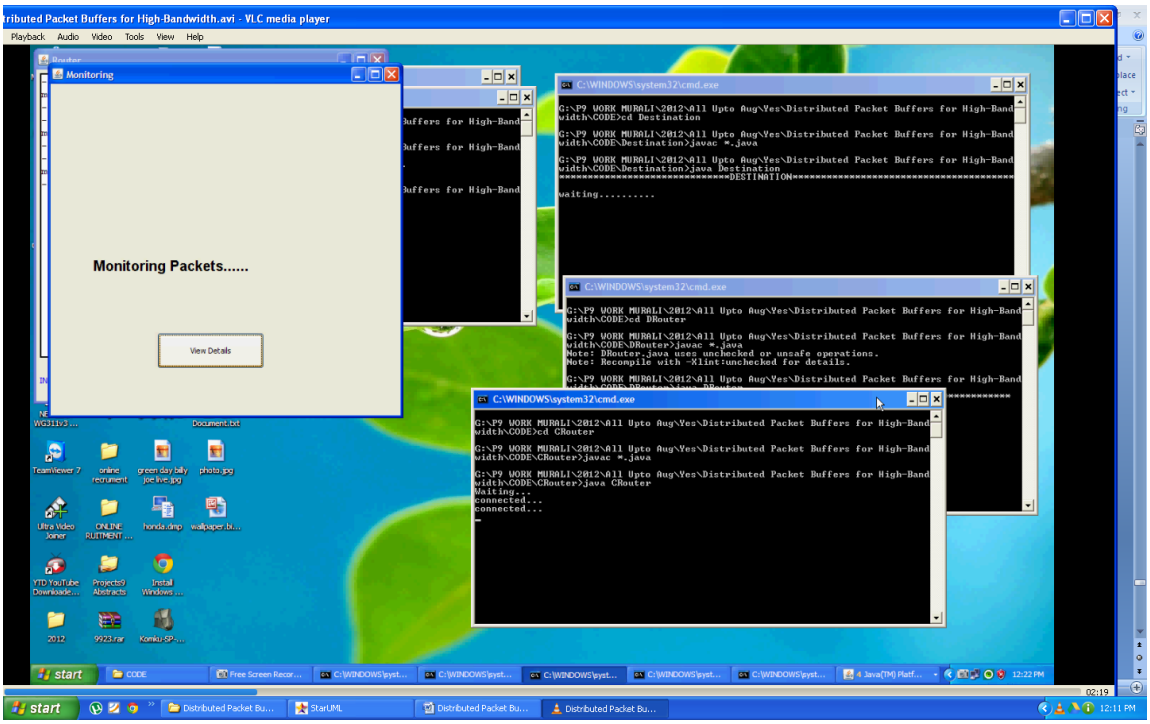
StarUML
12:10 PM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Monitoring
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DESTINATION
waiting.....
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Note: Recompile with -Xlint:unchecked for details.
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connected...
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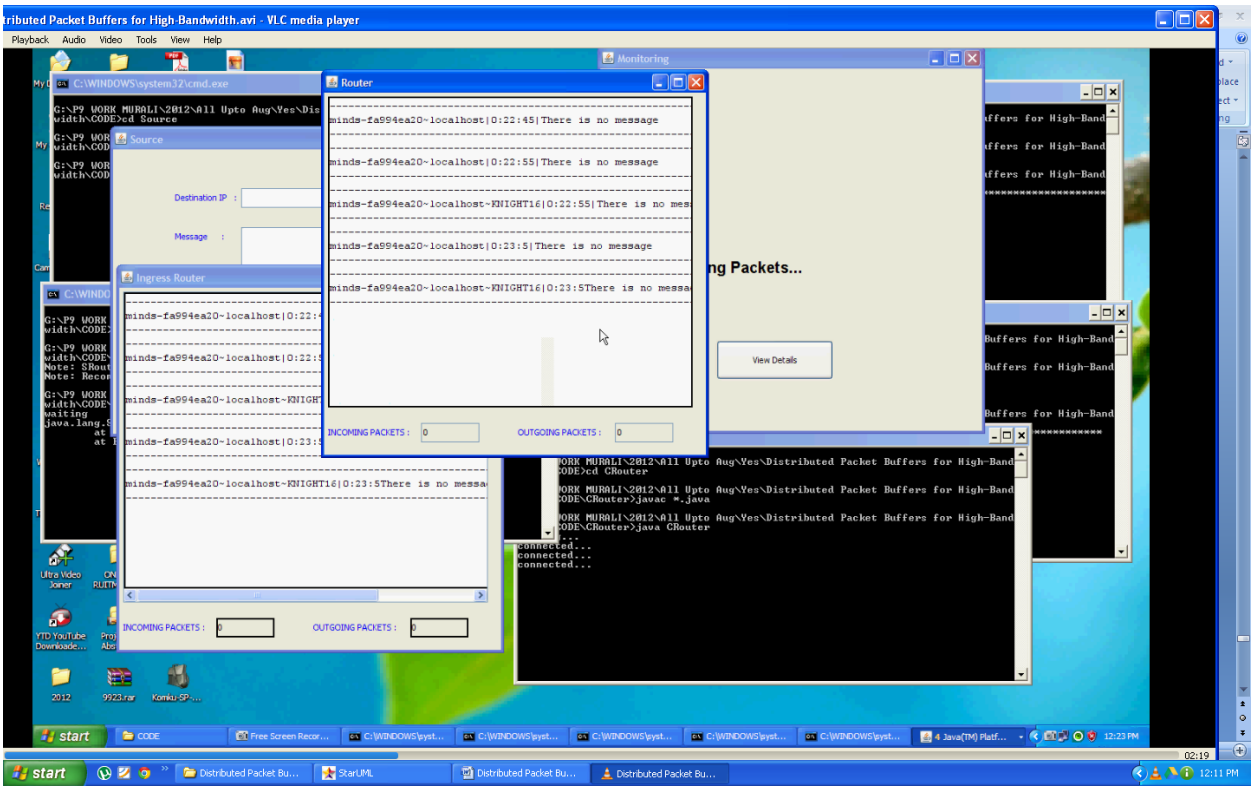
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Monitoring
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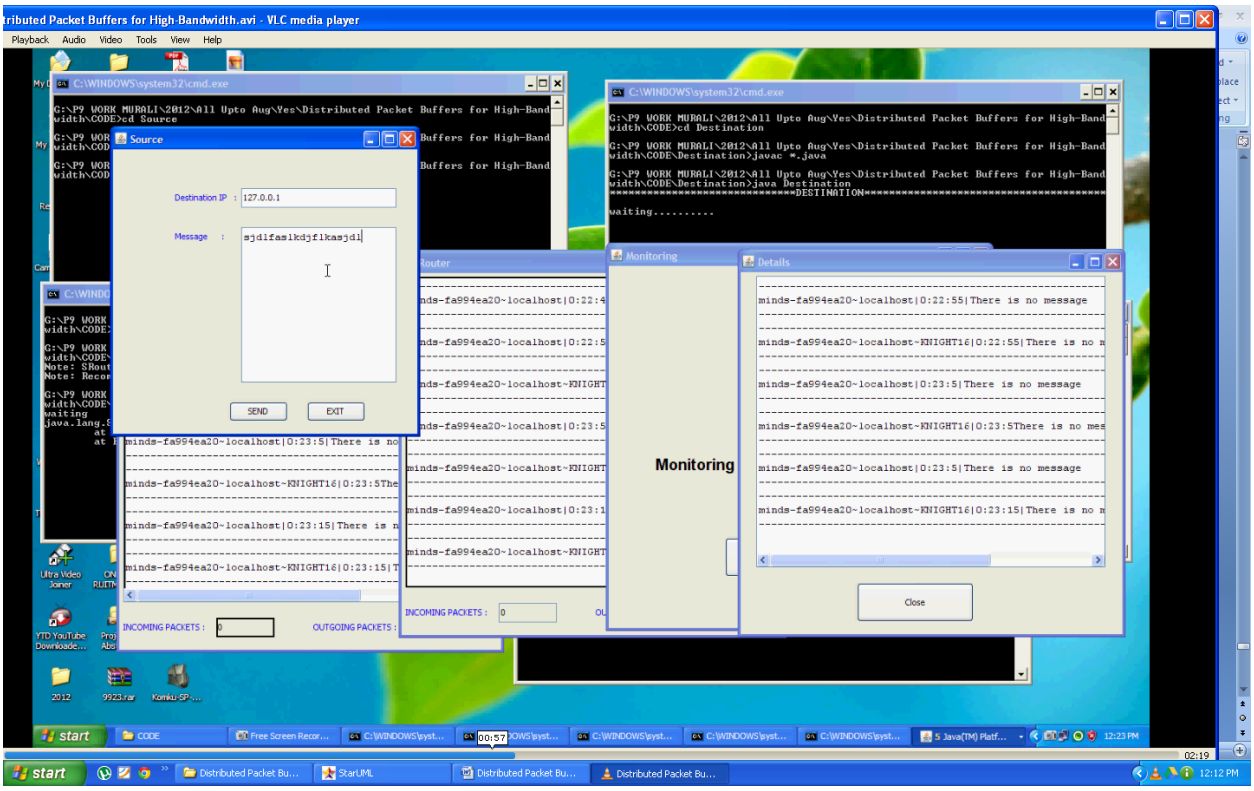
OUTGOING PACKETS :
View Details
start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Monitoring
Details
Close
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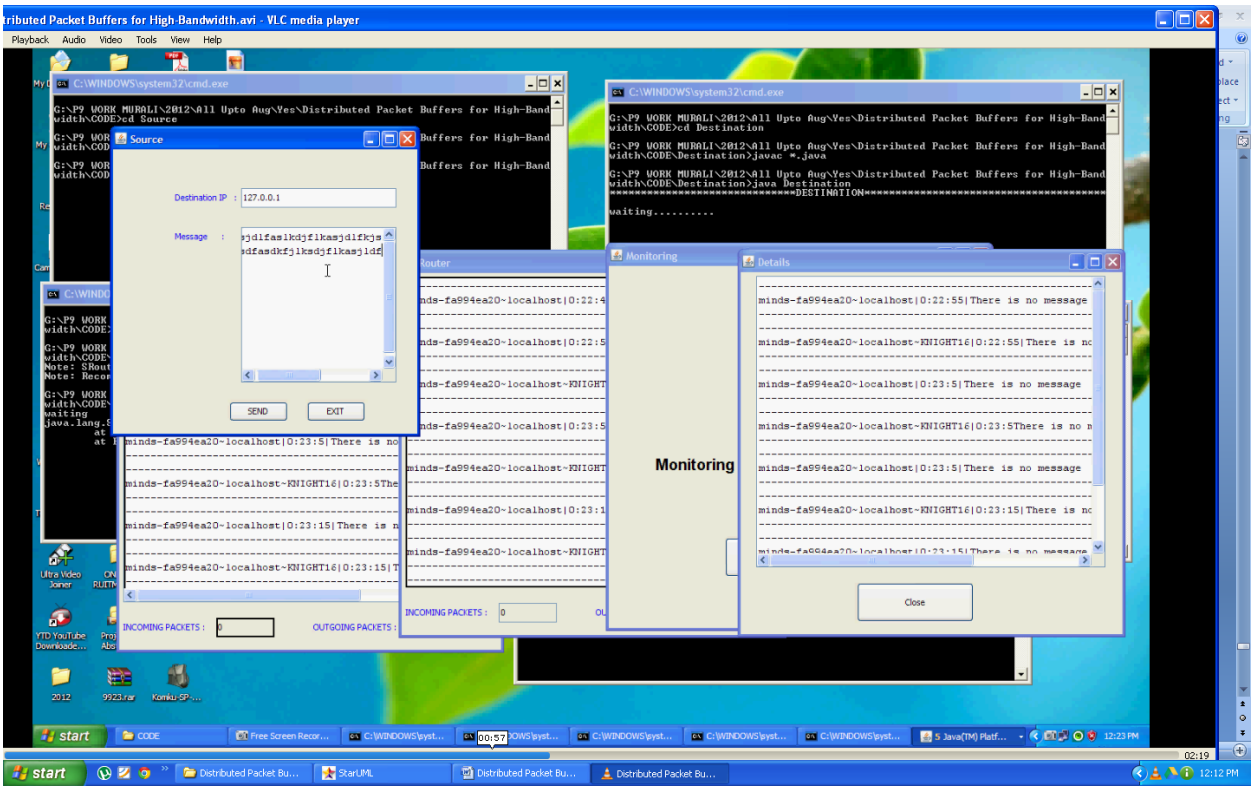
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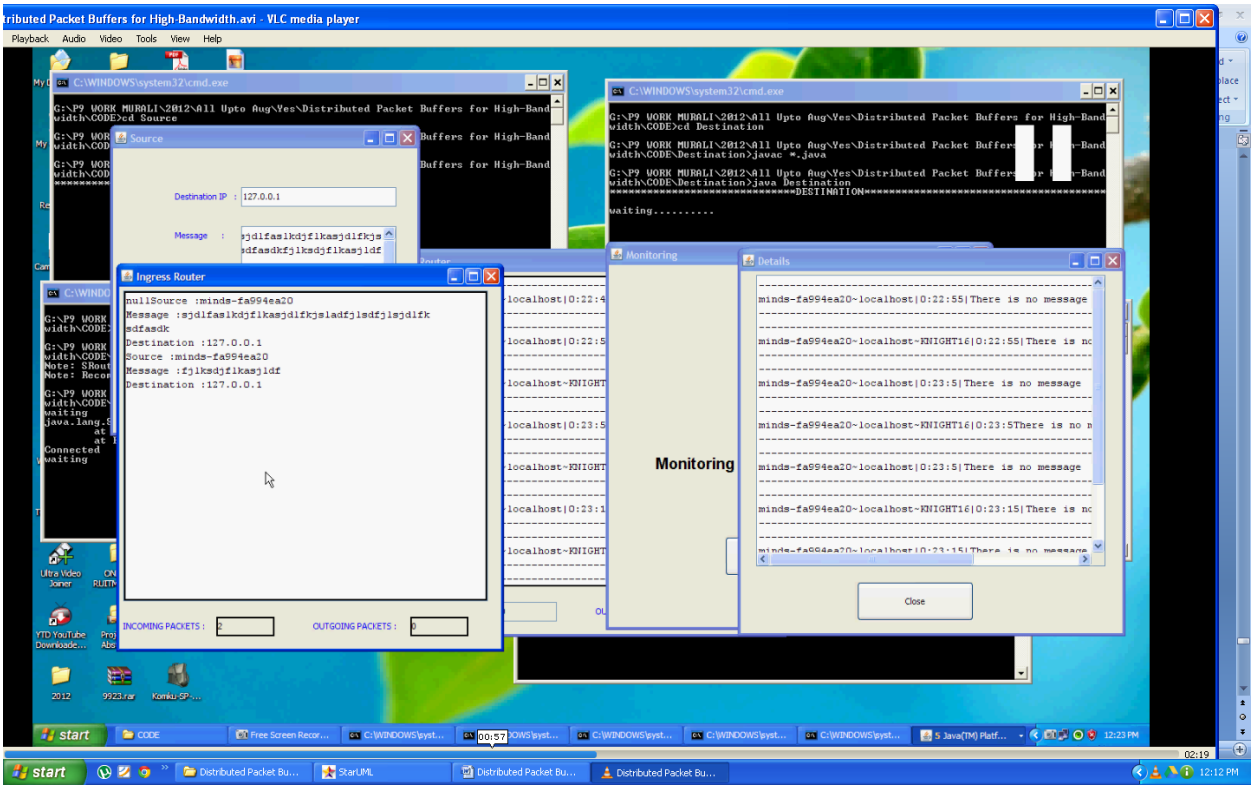
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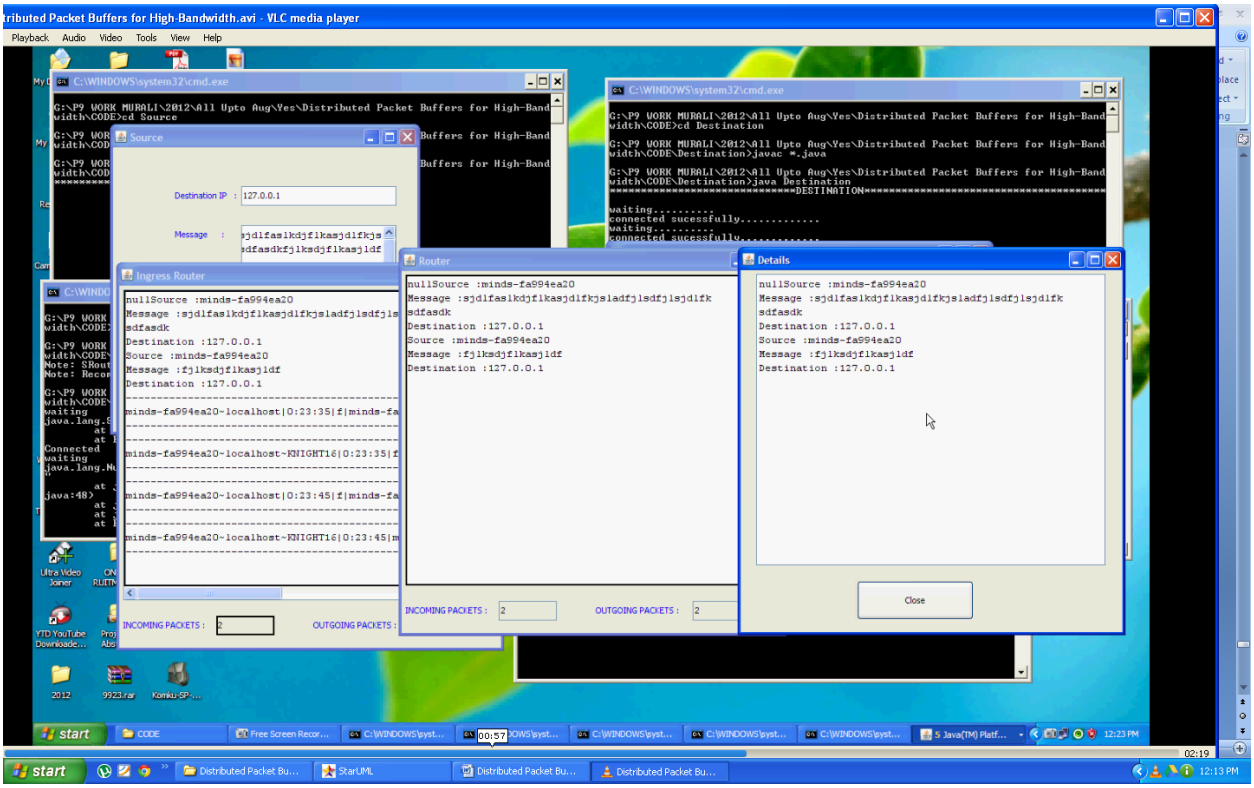
Message :sjdlfaslkdjflkasjdlfkjsladfjlsdfjlsjdlfk
sdfasdk
Destination :127.0.0.1
Source :minds-fa994ea20
Message :fjlksdjflkasjldf
Destination :127.0.0.1
Monitoring
Details
Close
INCOMING PACKETS :
OUTGOING PACKETS :
start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Message :sjdlfaslkdjflkasjdlfkjsladfjlsdfjlsjdlfk
sdfasdk
Destination :127.0.0.1
Source :minds-fa994ea20
Message :fjlksdjflkasjldf
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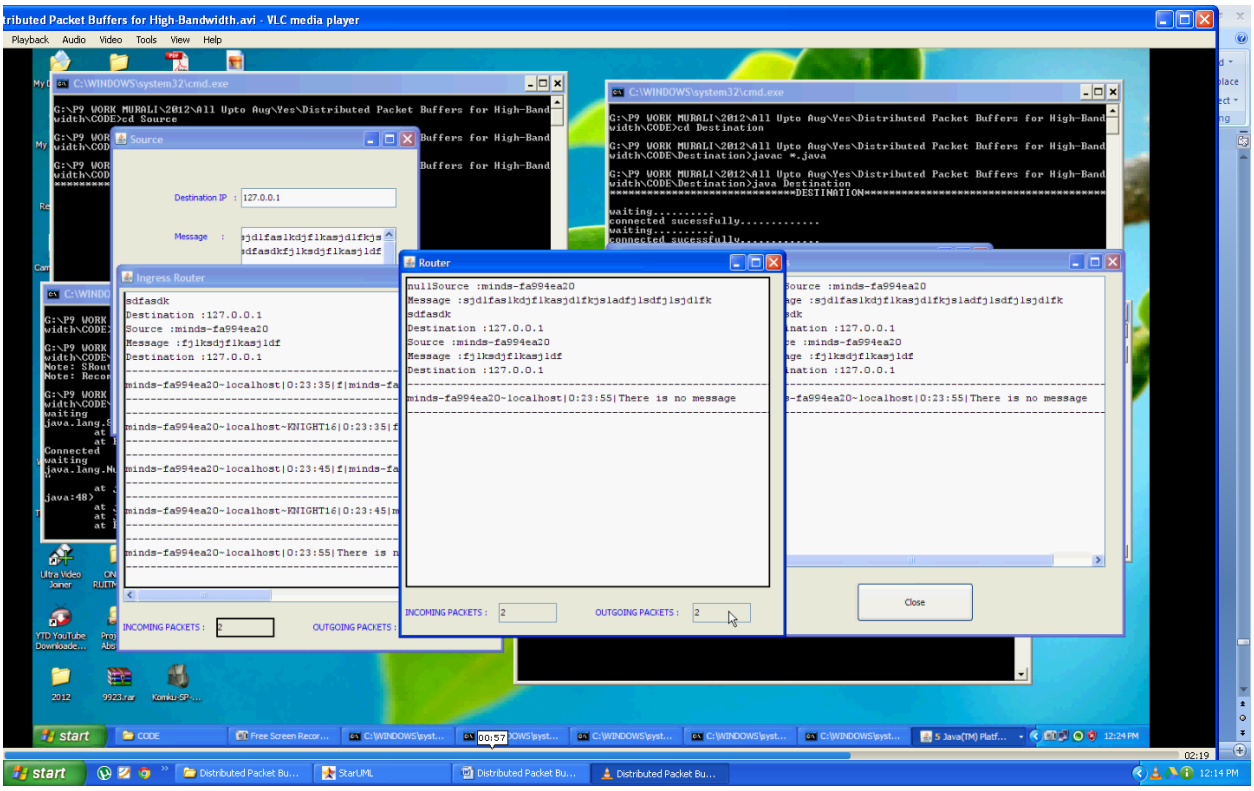
OUTGOING PACKETS :
Router
Details
Close
start
Distributed Packet Bu...
StarUML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Destination :127.0.0.1
INCOMING PACKETS :
OUTGOING PACKETS :
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Destination :127.0.0.1
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Message :fjlksdjflkasjldf
Destination :127.0.0.1
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OUTGOING PACKETS : 2
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width\CODE\Destination>javac *.java
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width\CODE\Destination>java Destination
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waiting.....
connected sucessfully.....
Close
start
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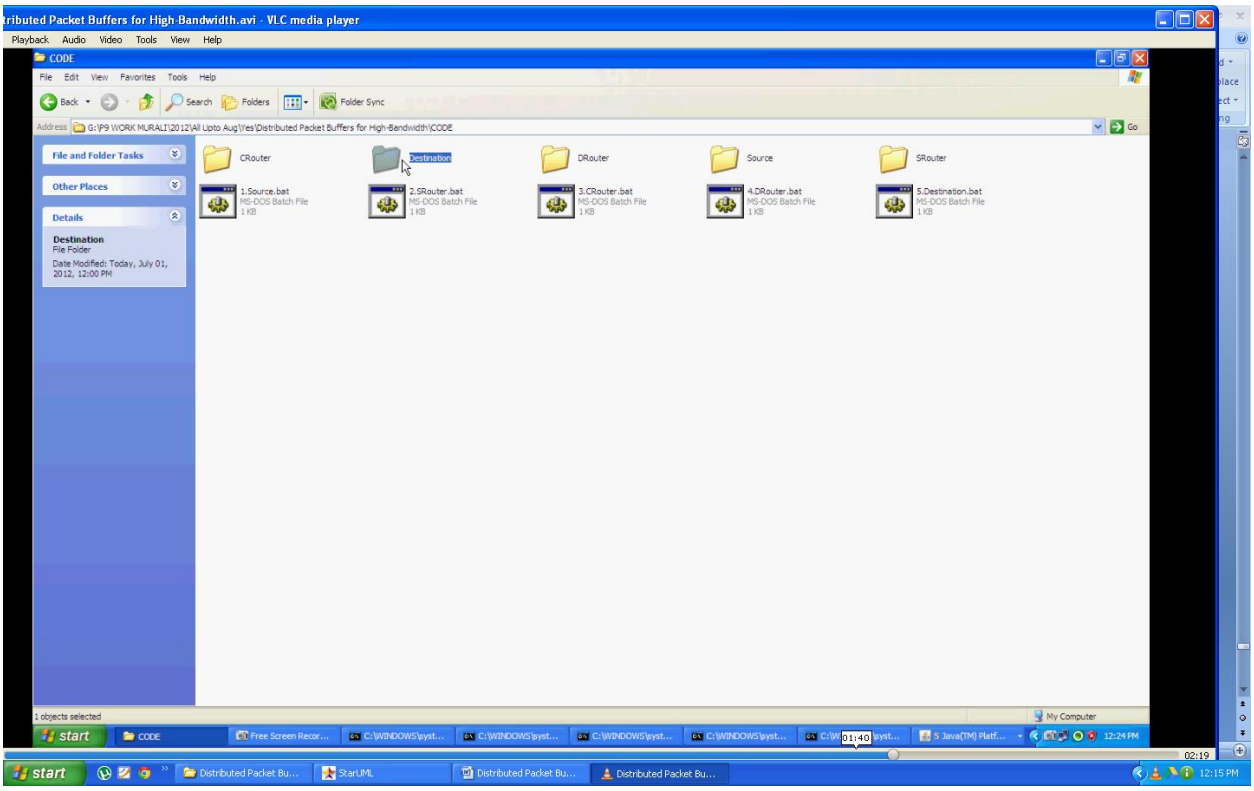
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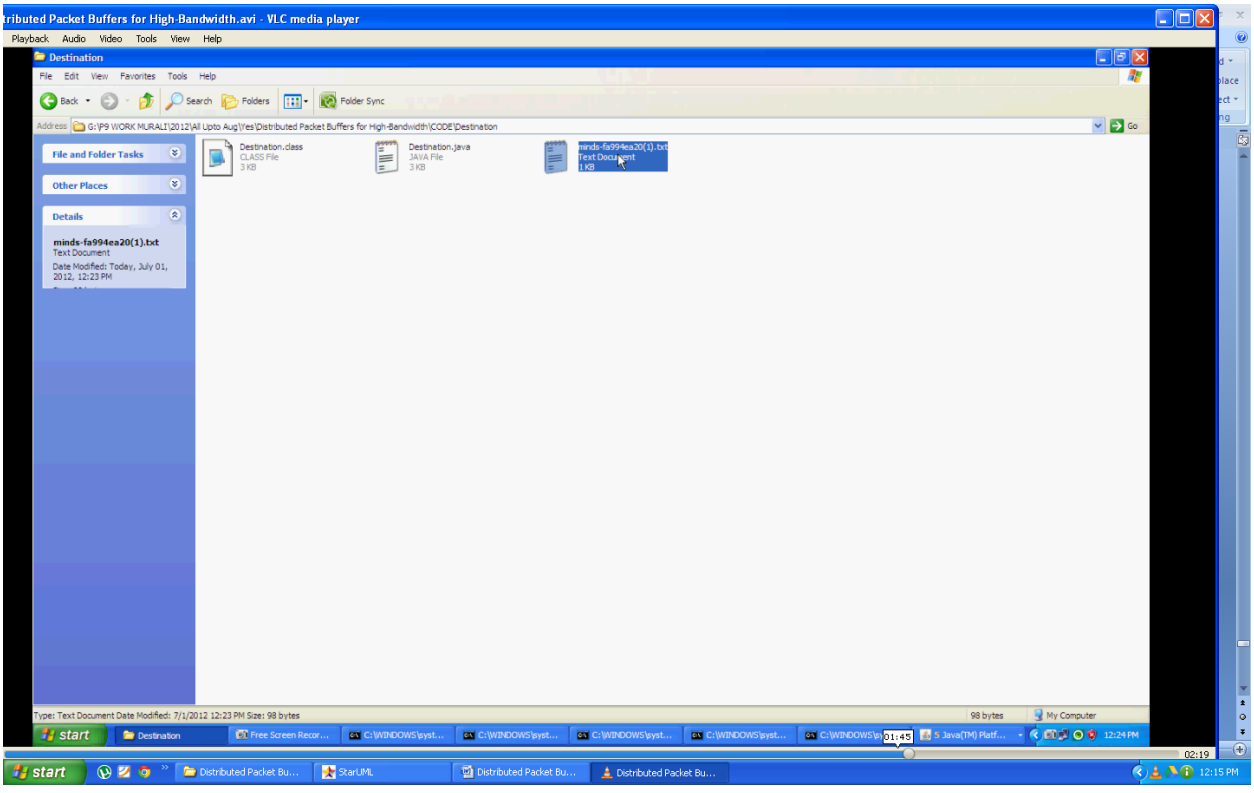
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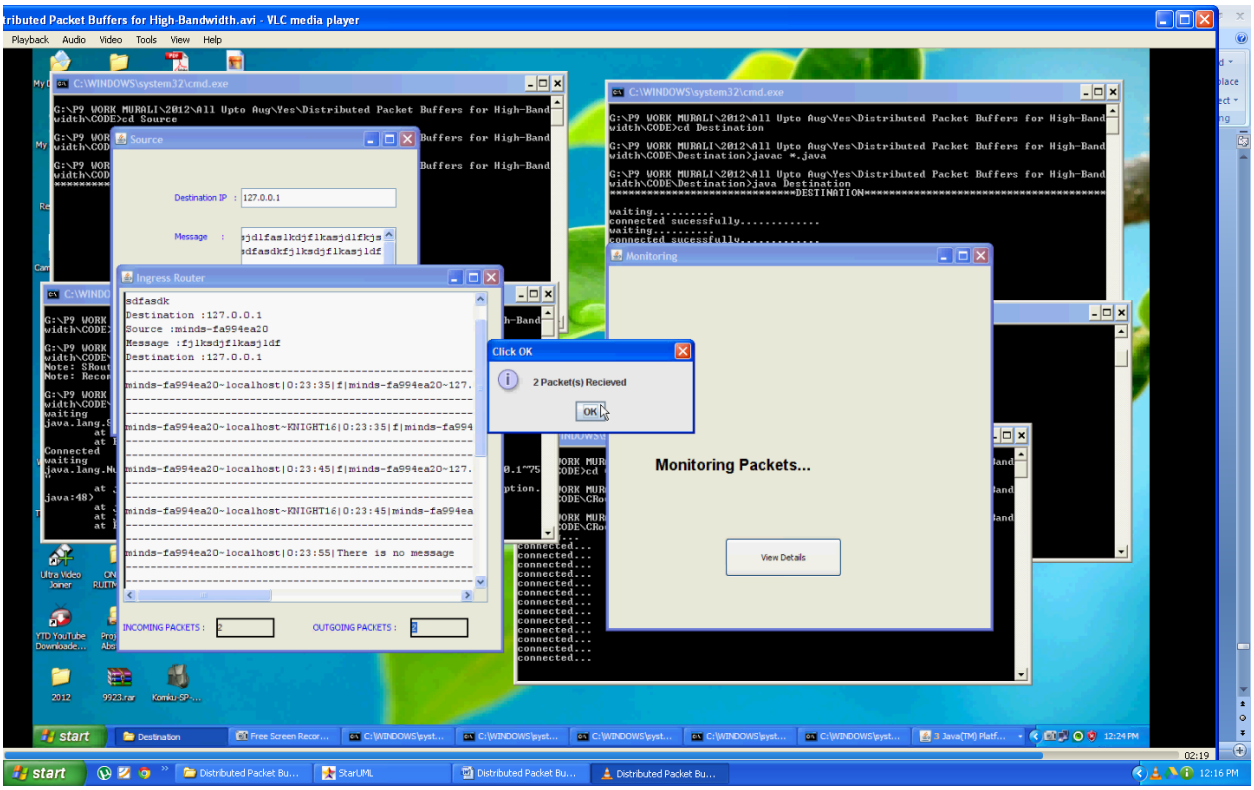

6. CONCLUSIONS AND FUTIRE WORK

Building packet buffers based on a hybrid SRAM/DRAM architecture while introducing minimum overhead is the major issue discussed in this paper. To distinctly increase the throughput and storage capacity of a packet buffer, a parallel mechanism using multiple DRAM chips should be deployed. Our analysis shows that previous algorithms make very little effects in exploring the advantage of parallel DRAMs leading to the requirement of large size SRAM and high time complexity in memory management. In this paper, we present a novel packet buffer architecture by using both fast batch load scheme and a hierarchal distributed structure. It reduces the requirement of SRAM size greatly. Both mathematical analysis and simulation results indicate that the proposed architecture provides guaranteed performance in terms of the low time complexity, short access delay, and upper bounded drop rate, when a small speedup is provided

7. REFERENCES

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